REMARKS

Claims 1, 4 and 5 have been amended. Claims 1-5 are currently pending in the application.

The Examiner rejected claims 1-5 under 35 USC § 102(b) as being anticipated by Miller (USPN 5,027,330). The claims have been amended to more clearly distinguish over the cited reference. Reconsideration is respectfully requested.

In particular, claims 1 and 4 have been amended to recite that the control unit for the memory system includes at least two counters that can be externally loaded *with variable, non-zero values,* respectively, by signals from the at least processors. These counters are illustrated in Figure 3 of the specification, for example, as counters CNT_W and CNT_R, used to address the memory block MB. No corresponding counters are believed to be found in Miller.

Independent claim 5 has been amended to recite that control commands associated with the set of input data and the set of output data select amongst a plurality of predefined addressing options. Examples of such addressing options are set forth in detail in Table 1 of the specification. Again, no corresponding teaching is believed to be found in Miller.

Accordingly, claim 1, 4 and 5 are believed to patentably define over the cited reference. Claims 2 and 3 are also believed to add novel and patentable subject matter to independent claim 1.

Withdrawal of the rejection and allowance of claims 1-5 is respectfully requested.

Respectfully submitted,

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